Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1-3. (Canceled)

4. (Previously presented) An encoder, comprising:

a state machine configured to generate a plurality of state bits, and

an interface configured to couple an input relating to one of the state bits into the state machine during a time period,

wherein the interface is configured to couple an input signal into the state machine during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

5-12. (Canceled)

13. (Currently amended) An encoder, comprising:

state generation means for generating a plurality of state bits, and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period,

wherein the interface means is configured to couple an input signal into the state generation means during a second time period, and couple a complement of said one of the state bits into the state ~~machine~~ generation means during the time period.

14-21. (Canceled)

22. (Previously presented) A transmitter, comprising:

an encoder comprising:

a state machine configured to generate a plurality of state bits, and

an interface configured to couple an input relating to one of the state bits into the state machine during a time period; and

an RF stage coupled to the encoder;

wherein the RF stage and the encoder are each an integral part of the transmitter and wherein the interface is configured to couple an input signal into the state machine during a second time period, and couple a complement of said one of the state bits into the state machine during the time period.

23-33. (Canceled)

34. (Currently amended) A transmitter, comprising:

an encoder comprising:

state generation means for generating a plurality of state bits, and

interface means for coupling an input relating to one of the state bits into the state generation means during a time period; and

an RF stage coupled to the encoder;

wherein the RF stage and the encoder are each an integral part of the transmitter and wherein the interface means ~~are~~ is configured to couple an input signal into the state generation means during a second time period, and couple a complement of said one of the state bits into the state ~~machine~~ generation means during the time period.

35-44. (Canceled)

45. (Previously presented) An encoder, comprising:

a state machine configured to generate a state, and

an interface configured to serially couple an input relating to a binary representation of the state into the state machine during a time period,

wherein the interface is configured to serially couple a plurality of input signals into the state machine during a second time period, and serially couple a complement of the binary representation of the state at the end of the second period into the state machine during the time period.

46-51. (Canceled)

52. (Currently amended) An encoder, comprising:

state generation means for generating a state, and

interface means for serially coupling an input relating to a binary representation of the state into the state machine during a time period,

wherein the interface means comprises a ~~switch~~ switching circuit configured to serially couple input signals into the state generation means during the second time period, and serially couple a complement of the binary representation of the state at the end of the second period into the state generation means during the time period.

53-57. (Canceled)

58. (Currently amended) A method of generating a signal, comprising:

generating a payload as a function of a state machine output;

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of state bits, the tail generation comprising serially feeding a complement ~~for~~ of each of the state bits for the binary representation of the state machine output at the end of the payload generation into the state machine.

59. (Currently amended) A method of generating a signal, comprising:

generating a payload as a function of a state machine output,

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding the most significant bit of the first state bits into the state machine during a first clock cycle to generate a ~~second~~ plurality of second state bits having a most significant bit, and feeding the most significant bit of the second state bits into the state machine during a second clock cycle.

60. (Original) The method of claim 59 wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

61. (Previously presented) A method of generating a signal, comprising:

generating a payload as function of a state machine output,

generating a tail as a function of a binary representation of the state machine output at the end of the payload generation, and

appending the tail to the payload,

wherein the state machine output comprises a plurality of first state bits having a most significant bit, the tail generation comprising feeding a complement of the most significant bit of the first state bits into the state machine during a first clock cycle to generate a plurality of second state bits having a most significant bit, and feeding a complement of the most significant bit of the second state bits into the state machine during a second clock cycle.

62. (Original) The method of claim 61, wherein the first state bits further comprise a least significant bit, and wherein the most significant bit of the second state bits is the least significant bit of the first state bits.

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63. (Currently amended) The encoder of claim 4, wherein the interface comprises a ~~switch~~switching circuit.

64. (Previously presented) The encoder of claim 4, further comprising an output including a second one of the state bits.

65. (Previously presented) The encoder of claim 64, wherein the interface comprises an output, the encoder output further including the interface output.

66. (Previously presented) The encoder of claim 4, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

67. (Currently amended) The encoder of claim 4, wherein the state machine ~~includes~~ comprises at least two delay registers configured to delay the plurality of state bits.

68. (Currently amended) The encoder of claim 67, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

69. (Currently amended) The encoder of claim 13, wherein the interface means comprises a ~~switch~~switching circuit.

70. (Previously presented) The encoder of claim 13, further comprising an output including a second one of the state bits.

71. (Currently amended) The encoder of claim 70, wherein the interface means comprises an output, the encoder output further including the interface means output.

72. (Previously presented) The encoder of claim 13, wherein the state generation means comprises a 2^P-state finite state machine where P is an integer greater than one.

73. (Currently amended) The encoder of claim 13, wherein the state generation means ~~includes~~ comprises at least two delay registers configured to delay the plurality of state bits.

74. (Currently amended) The encoder of claim 73, wherein the state generation means ~~includes~~ comprises an adder coupled to at least one of the delay registers.

75. (Currently amended) The transmitter of claim 22, wherein the interface comprises a ~~switch~~switching circuit.

76. (Previously presented) The transmitter of claim 22, wherein the encoder further comprises an output including a second one of the state bits.

77. (Previously presented) The transmitter of claim 76, wherein the interface comprises an output, the encoder output further including the interface output.

78. (Previously presented) The transmitter of claim 22, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

79. (Currently amended) The transmitter of claim 22, wherein the state machine ~~includes~~ comprises at least two delay registers configured to delay the plurality of state bits.

80. (Currently amended) The transmitter of claim 79, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

81. (Currently amended) The transmitter of claim 34, wherein the interface means comprises a ~~switchs~~switching circuit.

82. (Previously presented) The transmitter of claim 34, wherein the encoder further comprises an output including a second one of the state bits.

83. (Currently amended) The transmitter of claim 82, wherein the interface means comprises an output, the encoder output further including the interface means output.

84. (Previously presented) The transmitter of claim 34, wherein the state generation means comprises a 2^P-state finite state machine where P is an integer greater than one.

85. (Currently amended) The transmitter of claim 34, wherein the state generation means ~~includes~~ comprises at least two delay registers configured to delay the plurality of state bits.

86. (Currently amended) The transmitter of claim 85, wherein the state generation means ~~includes~~ comprises an adder coupled to at least one of the delay registers.

87. (Previously presented) The encoder of claim 45, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

88. (Currently amended) The encoder of claim 45, wherein the state machine ~~includes~~ comprises at least two delay registers configured to generate the state.

89. (Currently amended) The encoder of claim 88, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

90. (Previously presented) The encoder of claim 52, wherein the state generation means comprises a 2^P-state finite state machine where P comprises an integer greater than one.

91. (Currently amended) The encoder of claim 52, wherein the state generation means ~~includes~~ comprises at least two delay registers configured to generate the state.

92. (Currently amended) The encoder of claim 91, wherein the state generation means ~~includes~~ comprises an adder coupled to at least one of the delay registers.

93. (Currently amended) An encoder comprising:

a state machine configured to generate a plurality of state bits comprising a most significant bit and a second bit different from the most significant bit; and

an interface comprising at least one switching circuit and configured to couple an input representative of the most significant bit into the state machine during a time period and to couple a second input representative of the second bit into the state machine during a time period.

94-96. (Canceled)

97. (Currently amended) The method of claim 59, wherein:

generating a payload comprises providing data bits to the state machine through a switching ~~device~~circuit; and

generating a tail comprises providing state bits to the state machine through the switching ~~device~~circuit.

98. (Previously presented) The method of claim 59, wherein generating a tail comprises adding a least significant bit of the first state bits to the tail during the first clock cycle, and adding a least significant bit of the second state bits to the tail during the second clock cycle.

99. (Previously presented) The method of claim 59, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

100. (Currently amended) The method of claim 59, wherein the state machine ~~includes~~ comprises at least two delay registers configured to delay the plurality of first state bits.

101. (Currently amended) The method of claim 100, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

102. (Currently amended) The method of claim 61, wherein:

generating a payload comprises providing data bits to the state machine through a switching ~~device~~circuit; and

generating a tail comprises providing complement state bits to the state machine through the switching ~~device~~circuit.

103. (Previously presented) The method of claim 61, wherein generating a tail comprises adding a least significant bit of the first state bits to the tail during the first clock cycle, and adding a least significant bit of the second state bits to the tail during the second clock cycle.

104. (Previously presented) The method of claim 61, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

105. (Currently amended) The method of claim 61, wherein the state machine ~~includes~~ comprises at least two delay registers configured to delay the plurality of first state bits.

106. (Currently amended) The method of claim 105, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

107. (Previously presented) The encoder of claim 93, wherein the interface is configured to couple an input representative of the most significant bit into the state machine during a first time period, and couple a second input representative of the second bit into the state machine during a second time period different from the first time period.

108. (Previously presented) The encoder of claim 93, wherein:

the interface is configured to couple an input representative of the most significant bit into the state machine during a first time period; and

the encoder comprises an output configured to output a bit representative of a state bit other than the most significant bit during the first time period.

109. (Currently amended) The encoder of claim 93, wherein the ~~interface comprises a switch~~time period during which the second input representative of the second bit is coupled into the state machine is subsequent to the time period during which the input representative of the most significant bit is coupled into the state machine.

110. (Previously presented) The encoder of claim 93, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

111. (Currently amended) The encoder of claim 93, wherein the state machine ~~includes~~ comprises at least two delay registers configured to delay the plurality of state bits.

112. (Currently amended) The encoder of claim 111, wherein the state machine ~~includes~~ comprises an adder coupled to at least one of the delay registers.

113. (New) The encoder of claim 93, wherein the time period during which the second input representative of the second bit is coupled into the state machine is adjacent to the time period during which the input representative of the most significant bit is coupled into the state machine.

114. (New) An encoder comprising:

a state machine configured to generate a plurality of state bits comprising a most significant bit and a second bit different from the most significant bit; and

an interface configured to couple an input representative of the most significant bit into the state machine during a first time period, and couple a second input representative of the second bit into the state machine during a second time period different from the first time period.

115. (New) The encoder of claim 114, wherein the interface comprises at least one switching circuit through which data bits and state bits are provided to the state machine.

116. (New) The encoder of claim 114, wherein the second time period is subsequent to the first time period.

117. (New) The encoder of claim 114, wherein the second time period and the first time period are adjacent to each other.

118. (New) The encoder of claim 114, wherein the state machine comprises a 2^P-state finite state machine where P comprises an integer greater than one.

119. (New) The encoder of claim 114, wherein the state machine comprises at least two delay registers configured to delay the plurality of state bits.

120. (New) The encoder of claim 119, wherein the state machine comprises an adder coupled to at least one of the delay registers.